TEST STRUCTURE AND METHODOLOGY FOR SEMICONDUCTOR STRESS-INDUCED DEFECTS AND ANTIFUSE BASED ON SAME TEST STRUCTURE

ABSTRACT

A method for detecting semiconductor process stress-induced defects. The method comprising: providing a polysilicon-bounded test diode, the diode comprising a diffused first region within an upper portion of a second region of a silicon substrate, the second region of an opposite dopant type from the first region, the first region surrounded by a peripheral dielectric isolation, a peripheral polysilicon gate comprising a polysilicon layer over a dielectric layer and the gate overlapping a peripheral portion of the first region; stressing the diode; and monitoring the stressed diode for spikes in gate current during the stress, determining the frequency distribution of the slope of the forward bias voltage versus the first region current at the pre-selected forward bias voltage and monitoring, after stress, the diode for soft breakdown. A DRAM cell may be substituted for the diode. The use of the diode as an antifuse is also disclosed.